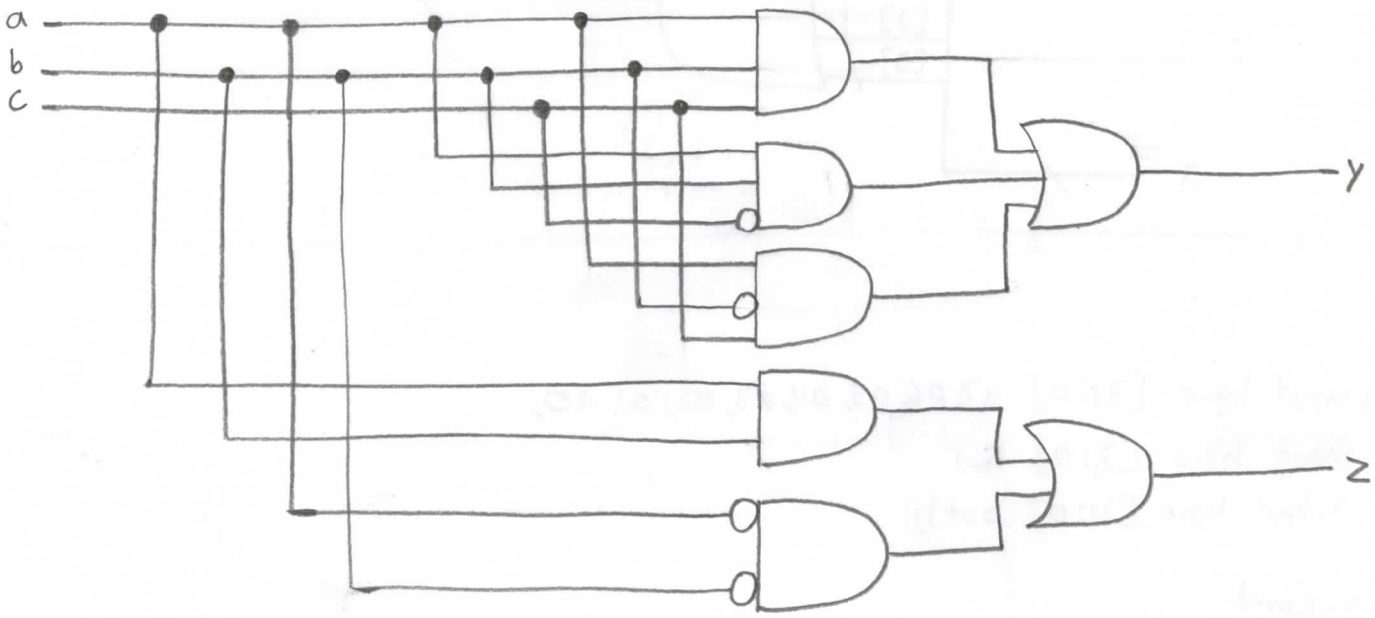
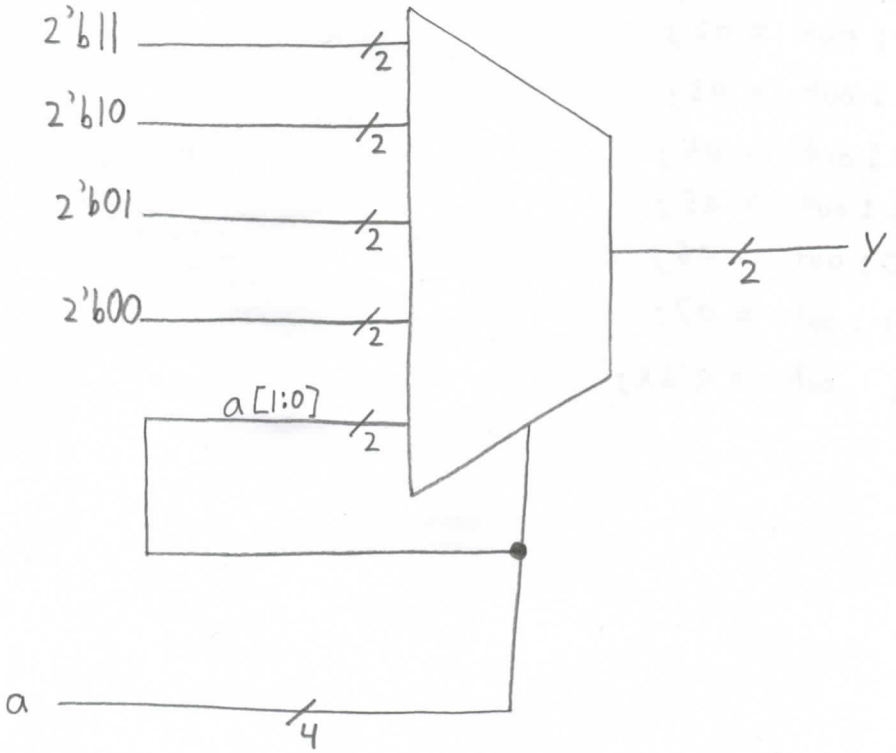
Name: Cole Shanks ID: 54950860

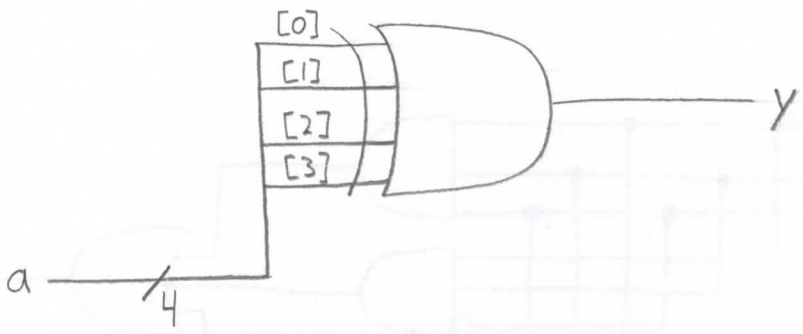
Q1



Q2



Q3



Q4

```
module mux(input logic [31:0] a7, a6, a5, a4, a3, a2, a1, a0,
           input logic [2:0] s,
           Output logic [31:0] out);

    always_comb
        case(s)
            3'b000: out = a0;
            3'b001: out = a1;
            3'b010: out = a2;
            3'b011: out = a3;
            3'b100: out = a4;
            3'b101: out = a5;
            3'b110: out = a6;
            3'b111: out = a7;
            default: out = 8'bx;
        endcase

endmodule
```

Q5

```
module pencoder(input logic a7, a6, a5, a4, a3, a2, a1, a0,
                output logic [2:0] out);

    always_comb begin
        if(a0) out = 1;
    else if(a1) out = 2;
    else if(a2) out = 3;
    else if(a3) out = 4;
    else if(a4) out = 5;
    else if(a5) out = 6;
    else if(a6) out = 7;
    else if(a7) out = 8;
    end
endmodule
```

Q6a

```
module 8reg(clk, d, q);
    input logic clk;
    input logic [7:0] d;
    output logic [7:0] q;

        always_ff @(posedge clk) begin
            q <= d;
endmodule
```

Q6b

```
module nine_reg(clk, rst, d, q);
    input logic clk, rst;
    input logic [8:0] d;
    output logic [8:0] q;

    always_ff @(posedge clk, posedge rst)
        if (rst) q <= 0;
        else     q <= d;
endmodule
```

Q6c

```
module n_reg(clk, rst, d, q);
    parameter N = 8;
    input logic clk, rst;
    input logic [N-1:0] d;
    output logic [N-1:0] q;

    always_ff@(posedge clk)
        if(rst) q <= 0;
        else    q <= d;
endmodule
```

Q6d

```
module async_reg(clk, rst, en, d, q);
    parameter N = 8;
    input logic clk, rst, en;
    input logic [N-1:0] d;
    output logic [N-1:0] q;

        always_ff @(posedge clk, posedge rst)
            if (rst) q <= 0;
            else if (en) q <= d;
endmodule
```

Q6e

```
Module latch(clk, d, q);
    input logic clk;
    input logic [7:0] d;
    output logic [7:0] q;

        always_latch
            if(clk) q <= d;
endmodule
```